Sub A8

ABSTRACT OF THE DISCLOSURE

A semiconductor device is provided with an SRAM memory cell. The semiconductor device includes a first gate-gate electrode layer, a second gate-gate electrode layer, a first drain-drain wiring layer, a second drain-drain wiring layer, a first drain-gate wiring layer and a second drain-gate wiring layer. The first drain-gate wiring layer and an upper layer and a lower layer of the second drain-gate wiring layer are located in different layers, respectively. The upper layer is provided above either an n-type well region or a p-type well region.